8.2

1

		■ [ ]
		■
		■
		■ DC105V
		■ AC152V
	CW	■ CW
	CCW	■ CCW
		■
		■
		■

2

“ DB ”

“ SB ”

53H DB

		3bit						
		Bit7	Bit6	Bit5				
	21	0	0	1		■ ■ ■	DB	
	22				0	■	DB	
	23				1	■	DB	
	24				2	■	DB	
	41	0	1	0	1	■	SB	
	42				2	■	DB	
	43					■	DB	
	44					■		
	45					■	SB	
	51					■	SB	
	52					■	SB	
	53					■	SB	
	55					■	DB	
	56					■	DB	
	61	0	1	1		■ DC	DB	
	62				1	■ DC	DB	
	63				1	■	SB	
	71				2	■	DB	3)
	72				1	■ ±12V	SB	
	73				2	■ +5V	DB	

		3bit					
		Bit7	Bit6	Bit5			
	84	1	0	0		■ ■	DB	
	85					■		
	A0	1	0	1	0	■	DB	
	A2				2	■	DB	
	A3				3	■	DB	
	A4				4	■ EEPROM	DB	
	AA				10	■	DB	
	AC				12	■	DB	
	AD				13	■	DB	
	AE				14	■	DB	
	AF				15	■	DB	

		3bit					
		Bit7	Bit6	Bit5			
	C1	1	1	0		■ 120%	DB	
	C2					■	DB	
	C3					■ 4	DB	
	C5					■	DB	
	D1					■	DB	
	D2				1	■	SB	
	D3				2	■	SB	
	DF				5	■	DB	
	E1	1	1	1	EEPROM	■ EEPROM	DB	
	E2				EEPROM	■ EEPROM		
	E3				1	■ CPU RAM		
	E4				2	■ CPU FIASH		
	E5				1	■		
	E6				2	■		
	E7					■		
	E8				CPU	■ CPU ASIC		
	E9					■		
	EE				1	■		
	EF				2	■		
	F1					■ CPU	DB	
	F2					■		

1)
2) S-RDY 1.5 2 PFDDLY GroupB ID16

3) 1s
4) ON
5)

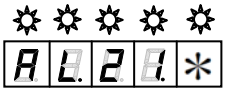
8.3

1

AL.85 *	2

0	(P-OFF)
2	(P-ON)
4	(S-RDY)
8	ON (S-ON)
9	(CSETRDY)
A	(EMR)
F	

2

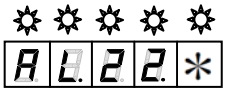


■ 21 ( )

	1	2	3	4
ON				

1	■ U V W U V W	■
2	■ U V W	■
3	■	■
4	■	■ 55

■ 22 (0)

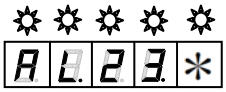


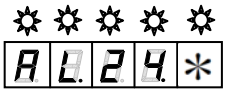
	1	2
ON		

1 ■	■
2 ■	■

■ 23 (1)

■ 24 (2)



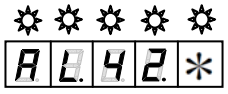


	1	2

1 ■	■
2 ■	■ ■

■ 41 (1)

	1	2	3	4	5	6	7
ON							

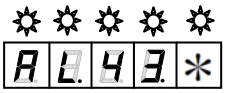


■ 42 (2)

	1	2	3	4	5	6	7
ON							

1	■	■
2	■ 50min−1 2	■ (TCMON) 2 2
3	■	■
4	■	■
5	■ U V W	■
6	■ U V W	■
7	■	■

■ 43 ( )

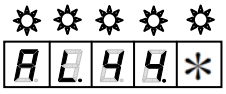


	1	2	3	4	5	6	7	8

1	■ ■	■ ■ ■ ■ ■
2	■	■
3	■	■
4	■	■ ■
5	■	■
6	■	■
7	■	■
8	■ ID02 (02)	■ ■ “ ”

ID02

■ 44



	1	2

1	■	■
2	■	■

■ 45

	1

1	■	■ ■

■ 51 ( )

	1	2	3	4

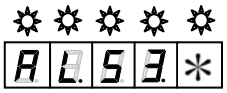
1	■	■
2	■	■ ■
3	■	■ 55
4	■	■ ■

■ 52 ( )

	1	2	3

1	■	■
2	■	■
3	■	■ 55

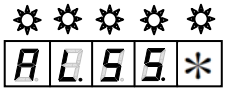
■ 53 ( )



	1	2

1 ■	■
2 ■	■

■ 55 ( )



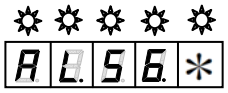
	1	2

1 ■	■ Group9 ID40 00 _Always_Disable
2 ■	■

	1	2	3

1 ■	■
2 ■	■ ■
3 ■	■

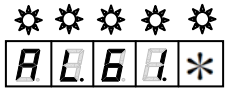
■ 56 ( )



	1	2	3	4
ON				

1	■ U V W U V W	■
2	■ U V W	■
3	■	■
4	■	■ 55

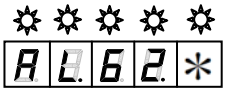
■ 61 ( )



	1	2	3	4

1	■	■
2	■	■
3	■	■
4	■ ■	■ ■ ■

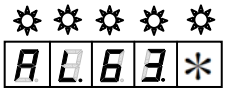
■ 62 ( )



	1	2	3	4	5

1	■	■
2	■	■
3	■	■
4	■ R S T	■ OFF R S T
5	■	■

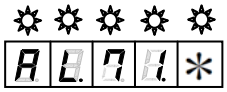
■ 63 ( )



	1	2	3

1	■ R S T	■
2	■	■
3	■	■ ID01 [ ]

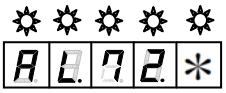
■ 71 ( )



	1	2	3

1	■	■
2	■	■
3	■	■

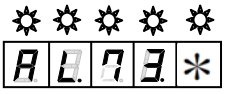
■ 72 (1)



	1	2

1 ■	■
2 ■	■ ■

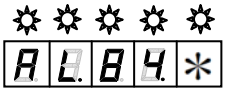
■ 73 (2)



	1	2

1 ■	■
2 ■	■

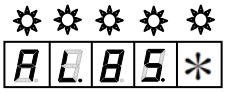
■ 84 ( )



	1	2	3

1 ■	
2 ■	■ ■
3 ■	■

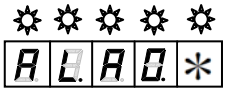
■ 85 ( )



	1	2	3

1	■	■
2	■	■
3	■	■

■ A0 (0)



	1	2

1	■	■
2	■	■ ■

■ A2 (2)

	1	2	3

1	■	■
2	■	■ ■
3	■	■

■ A3 (3)

	1	2	3

1	■	■
2	■	■ ■
3	■	■

■ A4 (4)

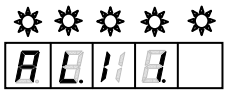
■ AA (10)

■ AC AF (12 15)

	1	2

1	■	■
2	■	■ ■

■ C1 ( )



	1	2	3	4
ON				

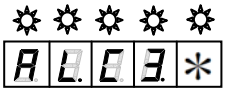
1	■	■
2	■	■
3	■	■ ■ ■
4	■ U V W	■

■ C2 ( )

	1	2	3
ON			

1	■ U V W	■
2	■ ( )	■ ( )
3	■	■ ■ ■ ■

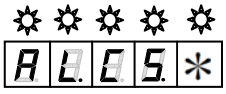
■ C3 ( )



	1	2	3

1	■	■ ■
2	■	■
3	■ ( )	■ ( )

■ C5 ( )

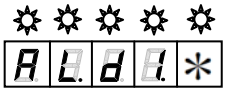


	1	2	3

1	■	■
2	■	■
3	■	■

,

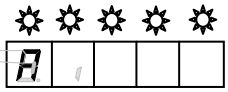
■ D1 ( )



	1	2	3	4	5	6	7	8	9	10	11	12
ON												

1	■	■
2	■	■
3	■	■ ( )
4	■	■
5	■ U V W	■
6	■ ( ) ( )	■
7	■ ■	■ ■
8	■ ( )	■ ( )
9	■	■
10	■	■
11	■	■
12	■	■

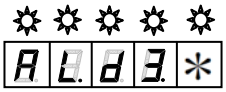
■ D2 (1)



	1

1	■	■ ■

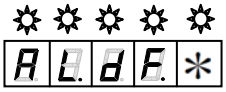
■ D3 (2)



	1	2

1	■	■
2	■	■

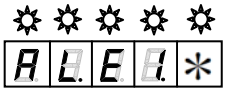
■ DF ( )



	1

1	■	■ ( )

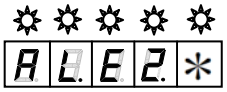
■ E1 (EEPROM)



	1

1	■	■

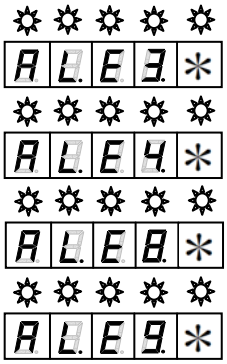
■ E2 (EEPROM)



	1	2

1	■ CPU EEPROM	■
2	■ EEPROM	■

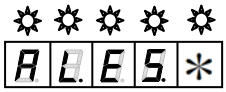
■ E3 (1)
■ E4 (2)
■ E8 (CPU)
■ E9 ( )



	1

1	■	■

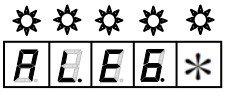
■ E5 (1)



	1	2

1	■	■
2	■	■

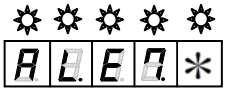
■ E6 (2)



	1	2

1	■ ■ ■	■ ■
2	■	■

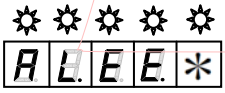
■ E7 ( )



	1	2

1	■ CPU EEPROM	■
2	■ EEPROM	■

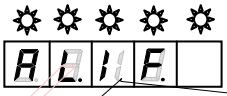
■ EE (1)



	1

1	■	■

■ EF (2)



	1	2

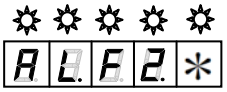
1	■	■ ■
2	■	■

■ F1 ( )

	1

1	■	■

■ F2 ( )



	1	2

1	■	■
2	■	■ ■